App. Serial No. 10/527,946
Docket No.: NL 020846 US

Remarks

The Final Office Action dated October 2, 2006 indicated two statutory rejections, specifically that: claims 1-5 stand rejected under 35 U.S.C. § 102(b) over Henrion (U.S. 6,198,360); and claims 6-15 stand rejected under 35 U.S.C. § 103(a) over Henrion in view of Albon *et al.* (U.S. 6,683,509).

Applicant respectfully traverses all of the Section 102(b) and Section 103(a) rejections based, *inter alia*, on the reasons previously presented in the Response dated 7/21/2006 which Applicant hereby incorporates by reference. The Examiner repeats the rejections from the previous Office Action and fails to adequately address Applicant's prior arguments. The M.P.E.P. dictates that the Examiner should take note of the applicant's arguments and answer the substance of them. *See* M.P.E.P. § 707.07(f). This is consistent with the purpose of aiding the applicant in judging the propriety of continuing the prosecution, as indicated in 37 C.F.R. § 1.104(a)(2) and 35 U.S.C. § 132. M.P.E.P. § 707.07(f) further urges that the Examiner state the reasons for his or her position (regarding Applicant's arguments) in the record.

The Examiner essentially repeats the rejections from the previous Office Action and fails to adequately respond to Applicant's arguments as required. For example, the Examiner fails to address Applicant's arguments regarding the lack of correspondence between the cited portions of the Henrion reference and the adder of the claimed invention. The Office Action cites to transistors Q9, Q10 as the modulator means, to transistors Q1-Q4 as the amplifier means, and to the nodes between the resistors and L1 and L2 as the adder of the claimed invention. However, the cited portions of the Henrion reference do not teach that the alleged adder (*i.e.*, the nodes) couple transistors Q9, Q10 to transistors Q1-Q4 as required by the claimed limitations, which require that the adder of the claimed invention couple the modulator means to the amplifier means (*see, e.g.*, FIG. 2). Moreover, the cited portions of the Henrion reference do not teach that the nodes provide feedback to the LC tank circuit as required by the adder of the claimed invention. Applicant submits that the Examiner's citation provided in support of providing feedback (e.g., Col. 3, lines 40-45) discusses feedback relative to FIG. 3, which has a configuration different from FIG. 2, and as such, does not provide clarification as to

how the Examiner is attempting to assert correspondence between the claimed limitations and the nodes asserted in the circuit of FIG. 2.

In another example, the Examiner fails to respond to Applicant's arguments regarding the lack of correspondence between the cited portions of the Henrion reference (*i.e.*, transistors Q5-Q8) and a buffer. Applicant submits that, contrary to the Office Action's assertion, the cited portions of the Henrion reference teach that these transistors are used as amplifiers. More specifically, Q5 and Q6 are used as an amplifier circuit with a gain that is dependent upon the voltage of VCONP, while Q7 and Q8 are used as an amplifier circuit with a gain that is dependent upon the voltage of VCONN. *See, e.g.*, FIGs. 1 and 2 and col. 2, lines 49-67.

In a further example, the Examiner fails to respond to Applicant's arguments regarding the previous Office Action's failure to provide adequate motivation or suggestion to modify the Henrion reference using the teachings of the Albon reference. In both the current and previous Office Actions the Examiner merely asserts that the Albon reference uses a VCO and a PLL and that the combination is conventional. Such unsupported assertions are insufficient to establish motivation or suggestion to combine as the Examiner has failed to show any motivation to use the specific teachings of the Henrion reference (FIG. 2) with the Albon reference. Moreover, Applicant respectfully traverses what appears to be an assertion by the Examiner that the FIG. 2 circuit of the Henrion reference is conventionally used by TV tuning circuits. More specifically, Applicant submits that the Examiner lacks support for the assertion that "these VCO oscillators are implemented conventionally with TV tuning circuits." Applicant notes that the VCO taught by the Albon reference (*e.g.*, FIG. 1) bears little resemblance to the circuit taught by FIG. 2 of the Henrion reference. Moreover, none of the cited portions of the references provide support for the assertion that the circuit of FIG. 2 of the Henrion reference is a conventional VCO used by TV tuners.

Without a correspondence to all of the claimed limitations and due to the Examiner's failure to adequately respond to Applicant's arguments as required by M.P.E.P. § 707.07(f), the Section 102(b) rejections of claims 1-5 and the Section 103(a) rejections of claims 6-15 are improper. Accordingly, Applicant requests that the rejections be withdrawn.

Applicant further traverses the Section 103(a) rejections of claims 7-15 because the Examiner fails to present a prima facie case of obviousness. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." *See* M.P.E.P. § 2143.03. The Examiner fails to cite to any portion of any reference that corresponds to numerous claimed limitations. For example, the Examiner fails address the limitations directed to a first high-impedance node that generates a first buffered signal from the inductive path and a second high impedance node that generates a second buffered signal from the capacitive path. Applicant notes, that the Examiner has merely asserted that high impedance is inherent and thus has not addressed how the cited references teach the claimed high impedance nodes for generating buffered signals from the respective paths. Therefore, the Section 103(a) rejections of claims 7-15 are improper and Applicant requests that they be withdrawn.

Moreover, the Examiner's assertion of inherency on page 3 of the current Office Action is improper and unsupported by the Henrion reference. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art" (*see, e.g.,* M.P.E.P § 2112(IV)). The Examiner merely states that "(w)ith regards the high impedance, this is inherent due to the fact that the oscillator output has to be isolated from loading effects that may affect the frequency when coupled to other elements" without providing any support for this statement from the references or otherwise. Accordingly, Applicant submits that the Examiner has in no way shown that high impedance nodes asserted by the Examiner are necessarily present in FIG. 2. Moreover, Applicant submits that the cited portions of the Henrion reference do not teach correspondence for high impedance nodes that generate buffered signals for both the capacitive path and resistive paths as required by the claimed limitations (*see, e.g.*, the asserted nodes between inductors L1 and L2). Accordingly, Applicant requests that the Section 103(a) rejections of claims 7-15 be withdrawn.

Applicant has made a minor amendment to claim 3 to correct a grammatical error. The amendment is not being made to overcome any issues of patentability or the rejections raised by the Examiner.

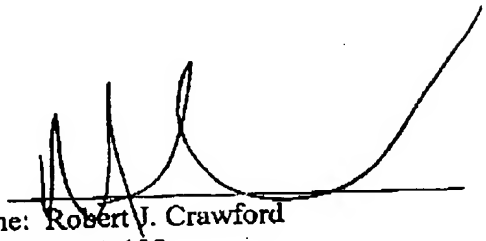
App. Serial No. 10/527,946
Docket No.: NL 020846 US

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of Philips Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
Philips Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 24738

By: 
Name: Robert J. Crawford
Reg. No.: 32,122
(VLSI.479PA)